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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,723	02/25/2002	Nigel D. Young	GB010051	8250

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/084,723	Applicant(s) YOUNG, NIGEL D.	
	Examiner Victor A Mandala Jr.	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 1 & 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed matter in claim 15 such as the further substrate having lines of weakness must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 10, & 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,821, 138 Yamazaki et al.

3. Referring to claim 1, a flexible matrix array device comprising: a thin film matrix circuit, (Figure 3 Col. 10 Lines 10-16), carried on the surface of a flexible substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), which matrix circuit, (Figure 3 shows a single pixel & Col. 6 Lines 43-45 and Col. 9 Lines 48-52), includes semiconductor devices, (Figure 2A #112, 115, & 110), arranged in a regular array, (Figure 3 shows a single pixel & Col. 6 Lines 43-45 and Col. 9 Lines 48-52), and occupying respective, discrete, areas of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), wherein selected regions of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), away from the areas occupied by the semiconductor devices, (Figure 2A #112, 115, & 110), comprises areas of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), at which flexing of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), occurs readily.

4. Referring to claim 2, A curved matrix array device comprising a thin film matrix circuit, (Figure 3 Col. 10 Lines 10-16), carried on the surface of a substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), which matrix circuit, (Figure 3 shows a single pixel & Col. 6 Lines 43-45 and Col. 9 Lines 48-52), includes semiconductor devices, (Figure 2A #112, 115, & 110), arranged in a regular array, (Figure 3 shows a single pixel & Col. 6 Lines 43-45 and Col. 9 Lines 48-52), and occupying respective, discrete, areas of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), wherein the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), comprises areas of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), at selected regions away from the semiconductor devices,

(Figure 2A #112, 115, & 110), and the curvature of the device is accommodated substantially by deformation at the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), at those regions.

5. Referring to claim 3, a flexible matrix array device, wherein the areas of weakness comprise locally thinner regions, (Figure 7 #701 & Col. 6 Lines 50-55), of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45).

6. Referring to claim 5, a flexible matrix array device, wherein the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), comprises a laminated structure, (Figure 3A), with at least two layers, (Figure 3A #120, Col. 9 Lines 18-19, & #101), and in which one layer is patterned to form the locally thinner regions, (Figure 7 #101).

7. Referring to claim 10, a flexible matrix array device, wherein the discrete areas of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), carrying the semiconductor devices, (Figure 2A #112, 115, & 110), are thicker, (Figure 7 sections that are between #701 & Col. 6 Lines 50-55), than the remaining areas of substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45).

8. Referring to claim 12, a flexible matrix array device, wherein the semiconductor devices, (Figure 2A #112, 115, & 110), comprises thin film transistors, (Figure 3 Col. 10 Lines 10-16).

9. Referring to claim 13, a flexible matrix array device, wherein the device comprises an active matrix display, (Figure 3 Col. 10 Lines 10-16), devices having an array of display pixels, (Figure 3 shows a single pixel & Col. 6 Lines 43-45 and Col. 9 Lines 48-52), and in which each semiconductor device, (Figure 2A #112, 115, & 110), is connected to a respective pixel electrode, (Figure 3 #118 & Col. 9 Lines 2-6), carried on the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45).

10. Referring to claim 14, a flexible matrix array device, wherein the device comprises an active matrix liquid crystal display device, (Figure 3 Col. 10 Lines 10-16), which includes a further flexible substrate, (Figure 3A #120, Col. 9 Lines 18-19), mounted to the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), carrying the matrix circuit, (Figure 3 shows a single pixel & Col. 6 Lines 43-45 and Col. 9 Lines 48-52), with liquid crystal material, (Col. 9 Lines 16-25), disposed between the substrates, (Figure 3 #101 & #120).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6, 8, 9, 11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,821, 138 Yamazaki et al.

11. Referring to claim 4, a flexible matrix array device, wherein the locally thinner regions are formed by selective etching of the substrate.

Initially, and with respect to claim4, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as

here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

12. Referring to claim 6, a flexible matrix array device, wherein the areas of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), comprise areas of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), at which the material of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), is rendered less stiff compared with the areas of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), occupied by the semiconductor devices, (Figure 2A #112, 115, & 110).
It is apparent that the thinner areas in a substrate would create less stiff areas. In Col. 6 Lines 50-55 it states that the grooves in the substrate are in a lattice shape and in Col. 9 Lines 48-52 it also states that the figures are only showing a single pixel of the matrix array. It is also apparent that in Figure 7 the substrate 101 defines grooves 701 and it would be obvious to one skilled in the art to see that the single pixel in Figure 3 is laid upon the substrate between the grooves, (Figure 7 #701), thus it is apparent that the less stiff areas of the substrate are not in the active areas of the matrix array.

13. Referring to claim 8, a flexible matrix array device, wherein the areas of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), extend as lines of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), between the area of the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), carrying the semiconductor devices, (Figure 2A #112, 115, & 110).
It is apparent that the weakness areas in a substrate would create lines of weakness. In Col. 6 Lines 50-55 it states that the grooves in the substrate are in a lattice shape and or stripes and in

Col. 9 Lines 48-52 it also states that the figures are only showing a single pixel of the matrix array. It is also apparent that in Figure 7 the substrate 101 defines grooves 701 and it would be obvious to one skilled in the art to see that the single pixel in Figure 3 is laid upon the substrate between the grooves, (Figure 7 #701), thus it is apparent that the weakness areas of the substrate are formed in a lattice shape which includes vertical and horizontal lines and the grooves are not in the active areas of the matrix array.

14. Referring to claim 9, a flexible matrix array device, wherein the semiconductor devices, (Figure 2A #112, 115, & 110), are arranged in an array of rows and columns and wherein the areas of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), comprise lines of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), extended across the array between rows and/ or columns of semiconductor devices, (Figure 2A #112, 115, & 110).

It is apparent that the weakness areas in a substrate would create lines of weakness. In Col. 6 Lines 50-55 it states that the grooves in the substrate are in a lattice shape and or stripes and in Col. 9 Lines 48-52 it also states that the figures are only showing a single pixel of the matrix array. It is also apparent that in Figure 7 the substrate 101 defines grooves 701 and it would be obvious to one skilled in the art to see that the single pixel in Figure 3 is laid upon the substrate between the grooves, (Figure 7 #701), thus it is apparent that the weakness areas of the substrate are formed in a lattice shape which includes vertical and horizontal lines and the grooves are not in the active areas of the matrix array.

15. Referring to claim 11, a flexible matrix array device, wherein the semiconductor devices, (Figure 2A #112, 115, & 110), each comprise a semiconductor film, (Figure 3 #103), formed into an island.

It is apparent that the weakness areas in a substrate would create lines of weakness. In Col. 6 Lines 50-55 it states that the grooves in the substrate are in a lattice shape and or stripes and in Col. 9 Lines 48-52 it also states that the figures are only showing a single pixel of the matrix array. It is also apparent that in Figure 7 the substrate 101 defines grooves 701 and it would be obvious to one skilled in the art to see that the single pixel in Figure 3 is laid upon the substrate between the grooves, (Figure 7 #701), thus it is apparent that the weakness areas of the substrate are formed in a lattice shape which includes vertical and horizontal lines and the grooves are not in the active areas of the matrix array. It also would be obvious to one skilled in the art to see that the active areas of the matrix would be in the shape of islands or mesas.

16. Referring to claim 15, a flexible matrix array device, wherein the further substrate, (Figure 3A #120, Col. 9 Lines 18-19), has lines of weakness, (Figure 7 #701 & Col. 6 Lines 50-55), formed therein.

Claim 15 discloses the claimed invention except for the further substrate having lines of weakness as seen in the substrate #101. It would have been an obvious matter of design choice to take the teachings of Yamazaki et al.s' lines of weakness in the substrate #101 and add it to the substrate of Yamazaki et al.s' substrate #120, since applicant has not disclosed that the lines of weakness in the further substrate solves any problem or is for any particular purpose and it appears that the invention would be performed equally well with the further substrate in a planar shape, but still made out of a flexible material as in Yamazaki et al., (Col. 9 Line 18).

Claim Rejections - 35 USC § 103

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,821, 138 Yamazaki et al. in view of U.S. Patent No. 5,821,688 Shanks et al.

17. Referring to claim 7, a flexible matrix array device, wherein the substrate, (Figure 3 & 7 #101 & Col. 6 Lines 43-45), comprises polymer material.

Yamazaki et al. teaches all of the claimed material in claim 7, but does not teach the substrate #101 to be made out of a polymer material. Shanks et al. teaches a flexible TFT matrix array with a substrate being made out of a polymer material, (Col. 5 Lines 40-44). It would be obvious to one skilled in the art to combine the teachings of Yamazaki et al. with the teachings of Shanks et al. because a polymer substrate would further allow the LCD matrix array to be more flexible.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
August 5, 2002

ALEXANDER O. WILLIAMS
PRIMARY EXAMINER